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L7: Entry 5 of 73 File: USPT Nov 18, 2003

DOCUMENT-IDENTIFIER: US 6650583 B2
TITLE: Test circuit device capable of identifying error in stored data at memory cell level and semiconductor integrated circuit device including the same

Detailed Description Text (128):
In the case of transferring test output data in a DDR mode (double data rate mode), data of the testing input/output pad changes synchronously with the rising and falling edges of test clock signal TCLK. In each of the test write data generating circuit and the test expected value data generating circuit shown in FIGS. 14 and 18, by providing two transfer paths and alternately operating the two transfer paths synchronously with the test clock signal, data can be transferred in the DDR mode in the data writing and reading modes.

L7: Entry 8 of 73 File: USPT Jun 3, 2003

DOCUMENT-IDENTIFIER: US 6574758 B1
TITLE: Testing a bus coupled between two electronic devices

Brief Summary Text (5):
In one embodiment, a bus having multiple lines and coupled between two electronic circuits (e.g. that communicate at double data rate abbreviated as "DDR") is tested by transmitting from a first circuit a test signal, and recognizing receipt of the test signal in a second circuit. Specifically, the second circuit compares a version of test signal received from the bus with a local copy of the test signal. If the received version does not match the local copy, a comparator in the second circuit indicates failure of receipt of the test signal.

Brief Summary Text (6):
In this embodiment, a sequence (over time, e.g., on successive edges of a clock signal in the case of DDR) of test signal is used to test the bus, and the second circuit specifically identifies the test signal that failed (from among other signals in the sequence) by generating an error signal. Such an error signal can simply indicate the location of the failed test signal in the sequence. In one implementation, the second circuit maintains a registrer, and bits in the register are accessed using the identity of the test signal as the address, and the values of the bits are set by the comparator.

Detailed Description Text (18):
Moreover, in the implementation illustrated in FIG. 4, a test signal checker 22 included in circuit 18 is similar to the above-described combination of test signal generator 10 and comparator 11 (FIG. 2), except for the differences related to DDR described above in reference to test signal generator 20. For example, test signal checker 22 simultaneously compares, in each cycle, two versions of n-bit signals received from bus 15 with the corresponding local copies generated from the pattern held in pattern register 23. Moreover, test signal checker 22 simultaneously supplies two status signals to status register 24.

L17: Entry 1 of 5 File: USPT Feb 10, 2004

DOCUMENT-IDENTIFIER: US 6691272 B2
TITLE: Testing of high speed DDR interface using single clock edge triggered tester data

Abstract Text (1):
A double data rate (DDR) circuit for testing of a high speed DDR interface using single clock edge triggered tester data. The DDR testing circuit includes a first register, a second register, and a multiplexer (MUX). A clock signal is fed to the first register and the MUX. The inverse of the clock signal is fed to the second register. A tester data signal is fed to the first register which generates a latched tester data signal which is fed to the MUX. The inverse of the latched tester data signal is fed to the second register which generates a transformed tester data signal which is fed to the MUX. The MUX generates a combination of the latched tester data signal and the transformed tester data signal for transmission as an applied test data signal. The resulting applied test data signal has double the data rate of the tester data signal upon which it is based.

Brief Summary Text (9):
A double data rate (DDR) circuit for testing of a high speed DDR interface using single clock edge triggered tester data is disclosed. The DDR testing circuit includes a first register, a second register, and a multiplexer (MUX). A clock signal is fed to the first register and the MUX. The inverse of the clock signal is fed to the second register. A tester data signal is fed to the first register which generates a latched tester data signal which is fed to the MUX. The inverse of the latched tester data signal is fed to the second register which generates a transformed tester data signal which is fed to the MUX. The MUX generates a combination of the latched tester data signal and the transformed tester data signal for transmission as an applied test data signal. The resulting applied test data signal has double the data rate of the tester data signal upon which it is based.

Drawing Description Text (2):
FIG. 1 is a block diagram of a DDR circuit according to the present invention for testing of a high speed DDR interface using single clock edge triggered tester data; and

Detailed Description Text (3):
Turning first to FIG. 1, a block diagram of a DDR circuit 10 according to the present invention for testing of a high speed DDR interface using single clock edge triggered tester data is shown. The DDR circuit 10 includes a first register 12, a second register 14, and a MUX (multiplexer) 16. Each register 12, 14 has a data input, a clock input, and an output. The clock input of the second register 14 is inverted. The MUX 16 has two data inputs, a clock input, and an output. The output of the first register 12 is connected directly to the first input of the MUX 16 and also through an inverter 18 to the data input of the second register 14. The output of the second register 14 is connected to the second input of the MUX 16. The DDR circuit 10 is preferably integrated with the chip to be tested. An external single clock edge triggered data generator (not shown) is connected to the input of the first register 12. The external data generator inputs a tester data signal which can take any of a number of well known desired patterns including complimentary and

shifted by n bits, among others. The output of the MUX 16 is connected to the internal data paths of the chip (not shown).

CLAIMS:

1. A double data rate (DDR) circuit for testing a high speed DDR interface using single clock edge triggered tester data, said circuit comprising: a first register having a data input, a clock input, and an output; a second register having a data input, a clock input, and an output, the data input of said second register being coupled to the output of said first register through an inverter; and a multiplexer (MUX) having a first data input, a second data input, a clock input, and an output, the first data input being coupled to the output of said first register to receive a first tester data signal, the second data input being coupled to the output of said second register to receive a second tester data signal.

8. A double data rate (DDR) device for testing a high speed DDR interface using single clock edge triggered tester data, said circuit comprising: means for generating a latched tester data signal from a tester data signal; means for generating a transformed tester data signal from the latched tester data signal by inverting and delaying by a half clock cycle the latched tester data signal; and means for generating an applied test data signal from the latched tester data signal and the transformed tester data signal.

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L13: Entry 7 of 11 File: USPT Jun 11, 1991

DOCUMENT-IDENTIFIER: US 5023590 A
TITLE: 17-bit cascadable comparator using generic array logic

Abstract Text (1):
A cascadable seventeen-bit self-testing comparator (20) is produced on a twenty-four pin GAL.RTM. 39V18 generic array logic chip by so interconnecting the data pins (1-17) with the logic macro cells (24a-h, 26a-i), and configuring the macro cells, that any data applied to the pins is registered in the macro cells (24a-h, 26a-i) upon pulsing the clock (35), and any exact coincidence of subsequent data with the registered data causes one of the macro cells (26j) to generate a match-indicating output (61).

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L13: Entry 11 of 11 File: DWPI Jun 11, 1991

DERWENT-ACC-NO: 1991-192706
DERWENT-WEEK: 199126
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TITLE: 17-Bit cascadable comparator using generic array logic - registers data applied to input pins in macro cell upon pulsing clock and any subsequent coincidence of data causes output

Basic Abstract Text (1):
The cascadable self-testing comparator chip has a generic logic array chip including a pulpable clock, a set of input pins, a set of logic macro cells, and a programmable crossbar switch for selectably interconnecting the same. Interconnections are programmed into the cross-bar switch to connect input pins to the macro cells, the macro cells being configured as registers storing data applied to the pins when the clock is pulsed, an additional macro cell has its input connected to said crossbar switch and having its output connected to an output pin.

L5: Entry 2 of 9 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6662136 B2
TITLE: Digital temperature sensor (DTS) system to monitor temperature in a memory subsystem

Detailed Description Text (18):
The circuit named BIST DGEN 39 provides Built In Self Test data generation. It is a pseudo-random pattern generator. In the embodiment, a series of Linear Feedback Shift Registers (LFSR) were used to provide a register bank equal to the width of the number of DQ pins. This generates a pseudo-random pattern which can be written to the DDR-II SDRAM 10, 20 during AC BIST (Alternating Current Built In Self Test).

Detailed Description Text (19):
The circuit named BIST AGEN 42 provides Built In Self Test address generation. In the embodiment, it is a register which increments through the address space of the DDR-II SDRAM during AC BIST.

Detailed Description Text (22):
Registers named System Data 41 (outputing to the data port of the SDRAMs 10, 20) and the command and address registers of System CMD/ADR 44 (outputting to the CMD/ADR port of the the SDRAMs 10, 20) are used during normal system operation to send data to and from the DDR-II SDRAMS. During normal operation, the master controller sends commands and addresses from System CMD/ADR 44 to a DDR-II SDRAM via CMD/ADR 34. During AC BIST, the master controller sends commands and addresses to a DDR-II SDRAM from BIST AGEN 42. During normal operation, the master controller sends data from System Data 41 to DDR-II SDRAM via the data DQ pins 31, 33, and vice-versa when sending data from DDR-II SDRAM to the system. During AC BIST, the master controller sends data to DDR-II SDRAM from BIST DGEN 39.

Detailed Description Text (23):
During AC BIST the master controller adjusts Vref to a specified value stored in the CFG REGS, according to the above previously described method of adjusting Vref by writing to DAC-Vref. The master controller then performs one or more iterations of AC BIST. The master controller first writes pseudo-random data to DDR-II SDRAM by seeding the LFSR of BIST DGEN from data in CFG REGS, and by initializing the starting address of BIST AGEN from the CFG REGS. The master controller signals BIST DGEN to shift its Linear Feedback Shift Registers (LFSR) when it signals BIST AGEN to increment its address. After all the data has been written to the DDR-II SDRAM, the master controller initializes BIST DGEN and BIST AGEN, and reads the data from one or more of the DDR-II SDRAMs. The data from the DDR-II SDRAM(s) and BIST DGEN are provided to BIST CMPR, and a compare is performed on the actual data received against the expected value provided by BIST DGEN. A count of failing bits and number of fails is maintained by BIST CMPR. Upon the completion of AC BIST, the master controller writes the results of the AC BIST from BIST CMPR to CFG REGS, which makes the information available to the system. Each write to memory, read from memory, and compare cycle can be considered an iteration at constant Vref. The master controller can then adjust Vref and repeat another iteration. The CFG REGS can be written in a manner so that the master controller steps through various settings of Vref, at each Vref setting performing a DDR-II write, read, and compare iteration.

Detailed Description Text (24):
AC BIST as described in this embodiment is run at the maximum speed of the DDR-II Interface ASIC DIA (30) and the DDR-II SDRAMs 10, 20. This provides the fastest possible method of running AC BIST in the memory sub-system.

L5: Entry 3 of 9 File: USPT Apr 8, 2003

DOCUMENT-IDENTIFIER: US 6545927 B2
TITLE: Integrated semiconductor circuit, in particular a semiconductor memory configuration, and method for its operation

Detailed Description Text (7):
In this case, it is assumed that the chip 1 is being operated at the wafer level with an interface functionality other than the normal operating mode as is also used by the user. This is referred to as the "changed operating mode" (for example mode two). In this case, various contactors, in general needle boards, can be used for the modes with different interface functionalities. This may be of interest, for example, for double data rate (DDR) chips, which are operated in the single data mode at wafer level in order to avoid the high operating frequency for DDR, for self-test solutions which are fitted on the chip in order to test the chip using low-cost test equipment, for RAMBUS which is tested in the DA mode at the wafer level, generally for performance reasons, in order to test a very fast semiconductor memory at low speed at the wafer level.

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L5: Entry 8 of 9 File: DWPI Jun 5, 2003

DERWENT-ACC-NO: 2003-658499
DERWENT-WEEK: 200362
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TITLE: Self-testable double data rate macro cell circuit for handheld computer, generates error condition when response signal of circuit do not have predetermined relationship with test double data rate signals

Basic Abstract Text (1):
NOVELTY - An evaluator compares the test double data rate (DDR) signal generated by a linear shift back register, with the response produced by the DDR circuit. A built-in self-test (BIST) controller generates an error condition, when the response signal do not have predetermined relationship with the test signals.

Basic Abstract Text (4):
ADVANTAGE - The DDR circuit is self-tested at high operating speed with greater flexibility.

Basic Abstract Text (5):
DESCRIPTION OF DRAWING(S) - The figures show the circuit block diagrams of the self-testable double data rate output macro cell. 1A, 1B/8

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L7: Entry 4 of 73 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6662136 B2
TITLE: Digital temperature sensor (DTS) system to monitor temperature in a memory subsystem

Detailed Description Text (18):
The circuit named BIST DGEN 39 provides Built In Self Test data generation. It is a pseudo-random pattern generator. In the embodiment, a series of Linear Feedback Shift Registers (LFSR) were used to provide a register bank equal to the width of the number of DQ pins. This generates a pseudo-random pattern which can be written to the DDR-II SDRAM 10, 20 during AC BIST (Alternating Current Built In Self Test).

Detailed Description Text (19):
The circuit named BIST AGEN 42 provides Built In Self Test address generation. In the embodiment, it is a register which increments through the address space of the DDR-II SDRAM during AC BIST.

L7: Entry 17 of 73 File: USPT Oct 8, 2002

DOCUMENT-IDENTIFIER: US 6463006 B2
TITLE: Semiconductor integrated circuit

Detailed Description Text (16):
FIG. 6 shows another example structure of the semiconductor integrated circuit (the semiconductor device) of the present invention. Referring to FIG. 6, there is shown a semiconductor device 10a having a clock synchronous memory 20a operable to perform a so-called DDR (double data rate) operation. The clock synchronous memory 20a, which is a functional circuit, receives from the outside of the device 10a the control signal CTL, the address signal ADR, the data input DI, and the external clock signal CLK, operates on the basis of the external information received (CTL, ADR, DI, and CLK), and provides the internal data output IDOUT in synchronization with both the rising and falling edges of the external clock signal CLK. A data output converting circuit 50a, which is a circuit means, responds to the test control signal TEST by converting the internal data output (two-valued logic signal) IDOUT which is variable at a predetermined variation frequency into the external data output (three-valued logic signal) DOUT which is variable at a less variation frequency than the two-valued logic signal. More specifically, based on the internal data output IDOUT provided from the clock synchronous memory 20a in synchronization with the external clock signal CLK, the data output converting circuit 50a generates the external data output DOUT in synchronization with the external clock signal CLK or in synchronization with a clock signal equivalent to the external clock signal CLK. A data output selecting circuit 60a, which is a circuit means, responds to the test control signal TEST by selecting between the external data output DOUT and the internal data output IDOUT and by providing, as the data output DO, either DOUT or IDOUT, whichever was selected, to the outside of the device 10a.

Detailed Description Text (23):
In the semiconductor device of FIG. 6, data, which vary in synchronization with both the rising and falling edges of the external clock signal CLK, are output in the normal mode (DDR) operation, as has been described above. On the other hand, in the test mode operation, the variation frequency that output data vary is cut in half, thereby making it possible to perform testing of the functional circuit with a low-speed test system. This therefore provides reductions in test system cost.